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In digital circuit design, register-transfer level is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals between hardware

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registers, and the logical operations performed on those signals. Register-transfer-level abstraction is used in hardware description languages like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived. Design at the RTL level

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Register-transfer level - Wikipedia

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Description. Register Transfer Level (RTL) is an abstraction for defining the digital portions of a design. It is the principle abstraction used for defining electronic systems today and often serves as the golden model in the

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design and verification flow. The RTL design is usually captured using a hardware description language (HDL) such as Verilog or VHDL.

Register Transfer Level (RTL) - Semiconductor Engineering

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Both are considered general-purpose digital design languages, each with subtle differences and advantages over the other.

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