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It is a programming language used to model a digital system by dataflow, behavioral and structural style of modeling. This language was first introduced in 1981 for the department of Defense (DoD) under the VHSIC program. Describing a Design. In VHDL an entity is used to describe a hardware module. An entity

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can be described using, Entity declaration

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VHDL Code: Library ieee;  
use ieee.std\_logic\_1164.all;  
entity half\_adder is  
port(a,b:in bit;

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sum,carry:out bit); end half\_adder; architecture data of half\_adder is begin sum<= a xor b; carry <= a and b; end data;

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VHDL is one of the commonly used Hardware Description Languages (HDL) in digital circuit design. VHDL stands for VHSIC Hardware Description Language. In turn, VHSIC stands for Very-High-Speed Integrated Circuit. VHDL was initiated by the US Department of Defense around 1981.



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